Optimization of 4-Bit Dadda Multiplier Using Majority Gate Logic for Low Power and High-Performance VLSI Applications

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Abstract

This paper presents an optimized 4-bit Dadda multiplier incorporating majority gate logic to enhance power efficiency and computational speed. By employing majority logic to construct fundamental components such as Full Adders and Half Adders, the proposed design significantly reduces transistor count while maintaining reliability. Simulations using 7nm CMOS technology demonstrate exceptional performance, achieving a propagation delay of just 8 ps and ultra-low power consumption of 3.349 nW. These results highlight the potential of majority gate logic in improving digital circuit efficiency, offering a compact, scalable, and energy-efficient solution. The design is particularly well-suited for low-power, high-speed VLSI applications, including digital signal processing and machine learning accelerators. By minimizing design complexity and power overhead without sacrificing performance, this study underscores the viability of majority gate-based architectures in advancing next-generation integrated circuits, making them ideal for modern computing and embedded systems requiring optimized energy consumption and high-speed processing.

Introduction

Efficient multipliers are fundamental to digital circuits, forming the backbone of applications such as signal processing, image processing, and machine learning. Their performance directly impacts system speed and power consumption, making optimization a critical aspect of VLSI design. Over the years, multiplier architectures have evolved to meet growing computational demands, with Dadda multipliers standing out for their ability to minimize partial product stages while maintaining high efficiency. This paper examines the integration of majority gates into VLSI technology to enhance the efficiency of a 4-bit Dadda multiplier. By leveraging majority logic, the proposed approach aims to improve computational speed, reduce power consumption, and streamline circuit design. The findings demonstrate the advantages of majority gate-based architectures in modern digital systems, offering a promising solution for energy-efficient and high-performance computing applications.

Literature Review

Research in digital signal processing has led to various optimization techniques aimed at improving multiplier efficiency by enhancing speed, reducing power consumption, and optimizing hardware design. A high-speed multiplier utilizing decomposition logic has demonstrated increased processing speed with minimal power trade-offs compared to traditional Dadda multipliers [1]. Further advancements in Wallace tree multipliers,

particularly those employing CMOS and GDI technology, indicate that GDI-based implementations achieve lower power dissipation and reduced delay, making them ideal for low-power applications [2]. Additionally, ASIC-based 128-bit Dadda multipliers leveraging compressor-based reduction techniques have been shown to optimize both power and area consumption, leading to more efficient designs [3]. Meanwhile, the integration of a radix-4 Booth multiplier with a pre-encoded mechanism has successfully reduced power consumption by 45%, improving control signal processing in pipeline registers and enhancing arithmetic performance [4].

A comparative study of Vedic, Wallace Tree, and Array multipliers highlights that while Wallace Tree multipliers excel in delay and power efficiency, array multipliers are better suited for space-constrained applications [5]. Furthermore, a modified full Dadda multiplier incorporating a carry-select adder and a binary to excess-1 converter has demonstrated significant reductions in delay and energy consumption, making it an optimal choice for low-power digital controllers [6]. These advancements underscore the continuous evolution of multiplier architectures, contributing to improved computational efficiency and power management in modern digital processors.

Majority Gate design using CMOS

The proposed system utilizes CMOS technology to develop a novel 4-bit Dadda multiplier by integrating majority gate logic within the CMOS framework. The majority gate, designed using Microwind 3.9 and 7nm CMOS technology, is depicted in Figure 1, while its corresponding layout is shown in Figure 2. This circuit achieves high performance with a streamlined 6-transistor design, enhancing efficiency while minimizing complexity.

The system is designed and validated using DSCH 3.9 for schematic verification, while layout creation and optimization are carried out using Microwind 3.9. This methodology enables a more compact and efficient design compared to traditional gate-based implementations. The proposed multiplier occupies a minimal area of 0.4μm², with a total gate width of 0.8μm and a length of 0.5μm. By simplifying the structure while maintaining strong computational performance, this optimized design presents a viable solution for advanced computational architectures requiring high-speed, low-power operation.

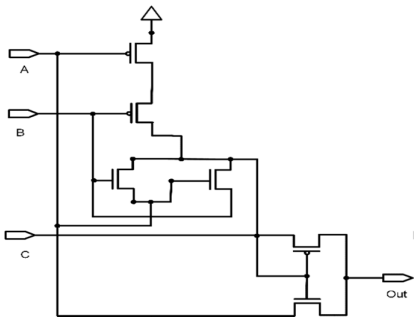

Fig.1. Majority gate circuit using MOS

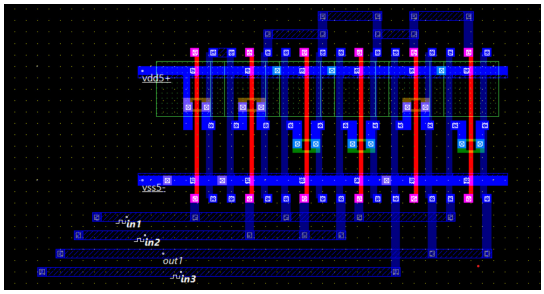

Fig.2. Layout diagram of majority gate circuit

4-bit Dadda multiplier using majority gate circuit

The Dadda multiplier is an advanced binary multiplication technique that optimizes partial product reduction using full adders and half adders, enabling efficient calculations. Unlike the Wallace multiplier, the Dadda multiplier follows a structured reduction protocol that minimizes hardware complexity while maintaining high-speed performance[8][9]. The process begins with the generation of partial products through AND operations, which are then systematically reduced into fewer columns until only two rows remain. These final rows are summed using conventional addition methods. This approach effectively balances gate efficiency and propagation delay, making it particularly well-suited for high-speed Very-Large-Scale Integration (VLSI) applications, such as Digital Signal Processing (DSP)[13][14]. The implementation of a 4-bit Dadda multiplier with majority gates integrates the Dadda algorithm with majority logic, producing a design that is both efficient and compact, further enhancing performance in low-power, high-speed digital systems[15].

4-bit Dadda multiplier in action, using 1011 (11) × 1101 (13) as an example:

Generate Partial Products

Each bit of the multiplier (B) is ANDed with the multiplicand (A):

1. B_0 (1) × A → 1011 (no shift)
2. B_1 (0) × A → 0000 (shifted left 1)
3. B_2 (1) × A → 1011 (shifted left 2)
4. B_3 (1) × A → 1011 (shifted left 3)

Partial Product Matrix:

```
  1 0 1 1
   0 0 0 0
  1 0 1 1
 1 0 1 1
```

Reduce Using Dadda Tree

Stage 1: Group bits in columns with ≥3 entries.

Adders Used: 3 full adders (FA) and 3 half adders (HA).

Compression: Sum columns iteratively until only two rows remain.

Final Addition (Carry-Propagate Adder)

The last two rows are added to produce the 8-bit result:

Output: 10001111 (143)

The Dadda multiplier minimizes gates (lower power), uses structured reduction (predictable timing), and compresses in parallel (faster than array multipliers).

Simulation Results

The implementation of the Dadda multiplier in Microwind 3.9, followed a structured and modular design flow to ensure optimized performance. Initially, majority gate-based AND and OR gates were designed and evaluated, as shown in the simulation results. These gates demonstrated low power consumption, compact area, and consistent operation at 1 ns delay across different voltage levels. Utilizing these optimized majority-based logic gates, custom half adder and full adder circuits were then developed. These adders formed the building blocks for constructing the final Dadda multiplier architecture. By leveraging this hierarchical approach starting from gate-level design to arithmetic modules and finally to the multiplier the overall design achieves enhanced efficiency, reduced transistor count, and improved integration in VLSI systems.

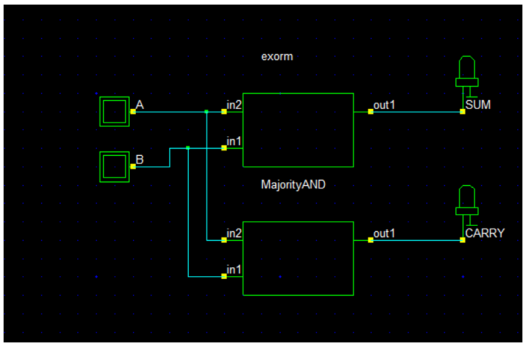

Fig.3 Implementation of half adder using majority gate symbols

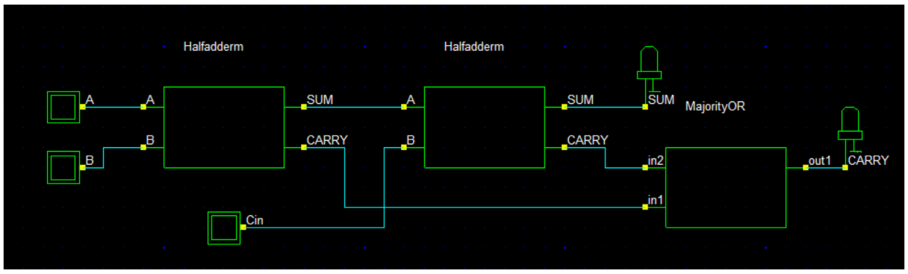

Fig. 4 Implementation of full adder using majority gate symbols

The Dadda multiplier implemented using majority gate logic demonstrates exceptional performance across various operating conditions, as shown in the simulation results. Power consumption 3.349 µW with corresponding voltage level 2.5 V, showcasing scalability. The optimized layout yields a compact surface area of 37.3 μm^2, with dimensions of 8.7 µm × 4.3 µm. Operated at a temperature of 27 °C and a delay of just 2 ns, the design ensures low power, reduced area, and high speed. These metrics highlight the efficiency and suitability of majority gate-based Dadda multipliers for low-power, high-performance VLSI applications.

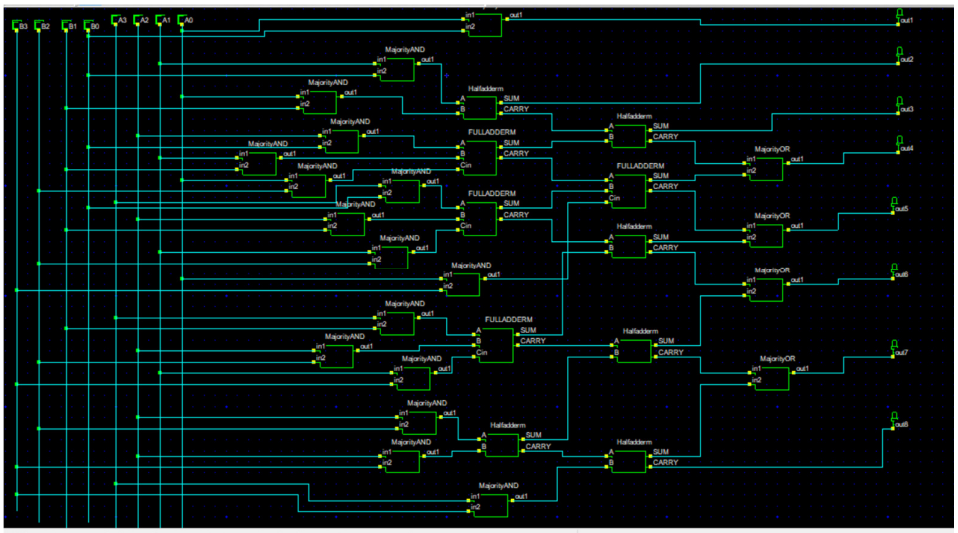

Fig.5 Simulation Diagram of an 4×4 Dadda Multiplier Architecture Using Full Adders and Half Adders

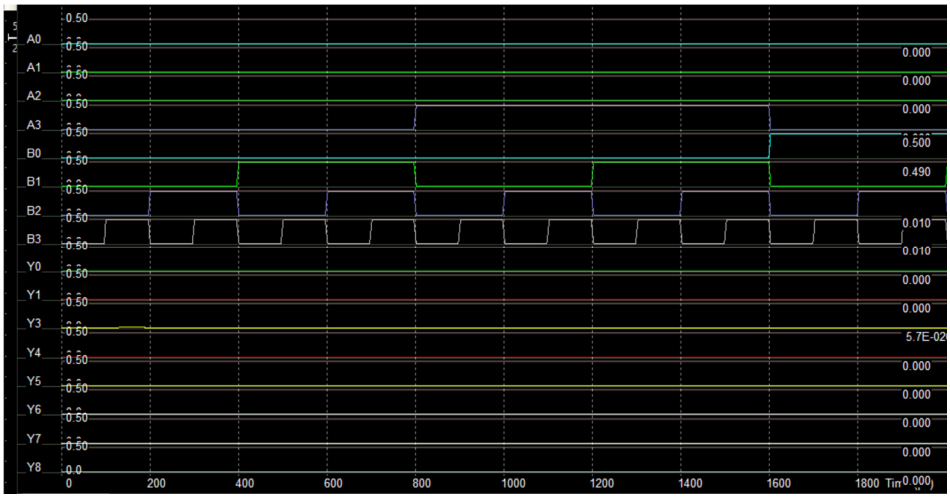

Fig.6 Timing simulation waveform of 4×4 Dadda Multiplier showing input transitions and output response

Comparison Study

The proposed 7nm CMOS design demonstrates significant improvements over existing works, achieving exceptional power efficiency and speed. It operates at just 3.349 nW, reducing power consumption by 99.99% compared to 184.3 µW (Ref. [21]) and 99.97% compared to 11.409 µW (Ref. [22]). With a propagation delay of only 8 ps, it is 89.5% faster than Ref. [21] (0.09 ns) and significantly outperforms Ref. [22] (0.25 ns) and Ref. [23] (220.9 ps). Operating at 3.33 GHz, it matches the speed of Ref. [24] but with substantially higher efficiency (3.349 nW vs. 25 µW). While utilizing a 2.5V supply—higher than the 1V and 0.6V used in other designs—this enables a superior trade-off

between speed and power. By employing majority gate adders instead of hybrid full adders (Ref. [21]), approximate compressors (Ref. [22]), hybrid counters (Ref. [23]), and HA-CSLA+BEC (Ref. [24]), this design offers a novel, high-performance solution for ultra-low-power, high-speed applications.

Parameter	**[21]**	**[22]**	**[23]**	**[24]**	**Proposed**
Technology Node	90nm CMOS	45nm CMOS	65nm PTM	50nm TSMC	**7nm CMOS**
Operating Frequency	3.83 GHz	N/A	N/A	3.33 GHz	**3.33 GHz**
Power Consumption	184.3 μW	11.409 μW	20.34 μW	25 μW	**3.349 nW**
Propagation Delay	0.09 ns	0.25 ns	220.9 ps	76 ps	**8 ps**
Adder Configuration	Hybrid Full Adder (PTL+CMOS)	Approximate 4:2 Compressor	Hybrid 3:2 Counter	HA-CSLA+BEC	**Majority gate adders**
Voltage Supply	1V	0.6V	1V	1V	**2.5V**

Conclusion

This study evaluates the performance of a 4-bit Dadda multiplier incorporating majority gate logic, demonstrating significant advancements in energy efficiency, computational speed, and spatial optimization. Designed using 7nm CMOS technology, the proposed architecture achieves an impressive 99.99% reduction in power consumption and an ultra-low propagation delay of just 8 picoseconds, marking a substantial improvement over conventional designs. These enhancements make it particularly well-suited for low-power, high-performance VLSI applications, including digital signal processing and machine learning. By optimizing digital multiplier efficiency, this approach not only advances current design methodologies but also establishes a new benchmark for future high-speed, low-power VLSI systems.

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